Atlas CSC ASMII Critical Design Review

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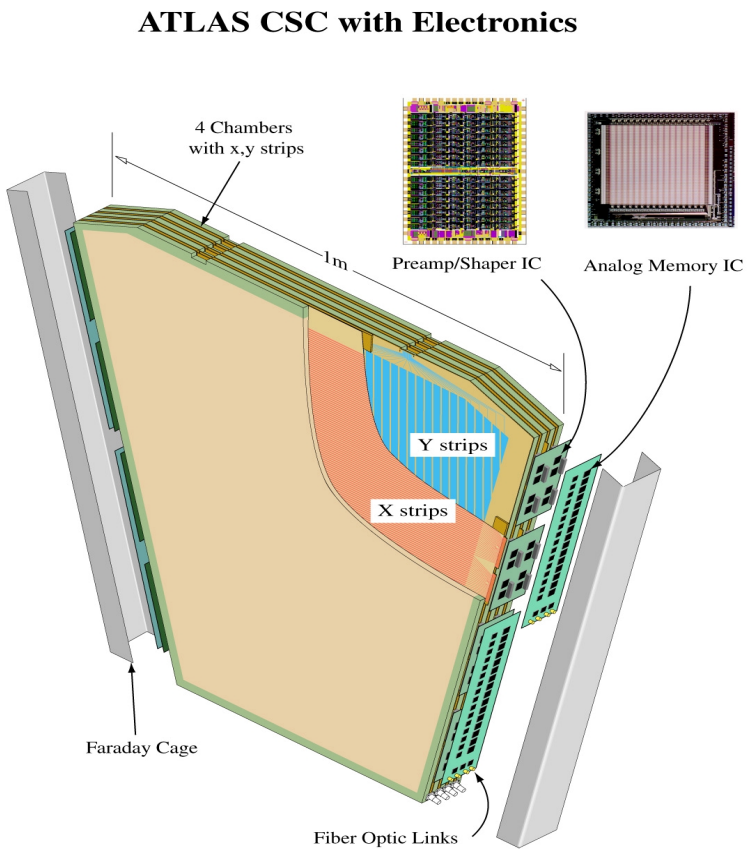
Overview

1. Introduction to ASMII
2. CSC electronics specifications
3. Design Evolution
4. Final design
5. ASMII test results
6. ROD Interface
7. COTS and ASIC qualification status and plans
8. Production, QA/QC plans
9. ASMII test procedures
10. Production Schedule
11. Conclusion

ATLAS CSC with Electronics



ASMII FACTS

- 5 boards per chamber
  - 4 x-strip (2 per side)
  - 1 y-strip
- 160 boards per system (128 x-strip, 32 y-strip)
- 192 Channels per ASMII

CSC electronics specifications

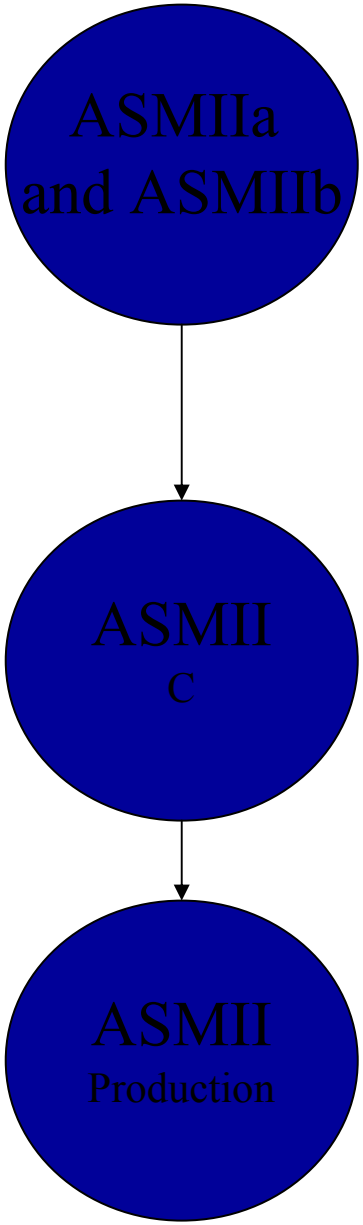
$$ENC \leq 0.5\ fC = 3100\ e-$$

Trigger rate 100KHz

KEY MILESTONES

- January 2001 :ASMII-a prototype
- February 2002 :ASMII-b prototype
- December 2002 :Critical Design Review
- August 2003 :ASMII-C prototype
- May 2004 :System integration test
- June 2004 :Production readiness review
- October 2004 :ASMII Production complete

ASMII Design Evolution



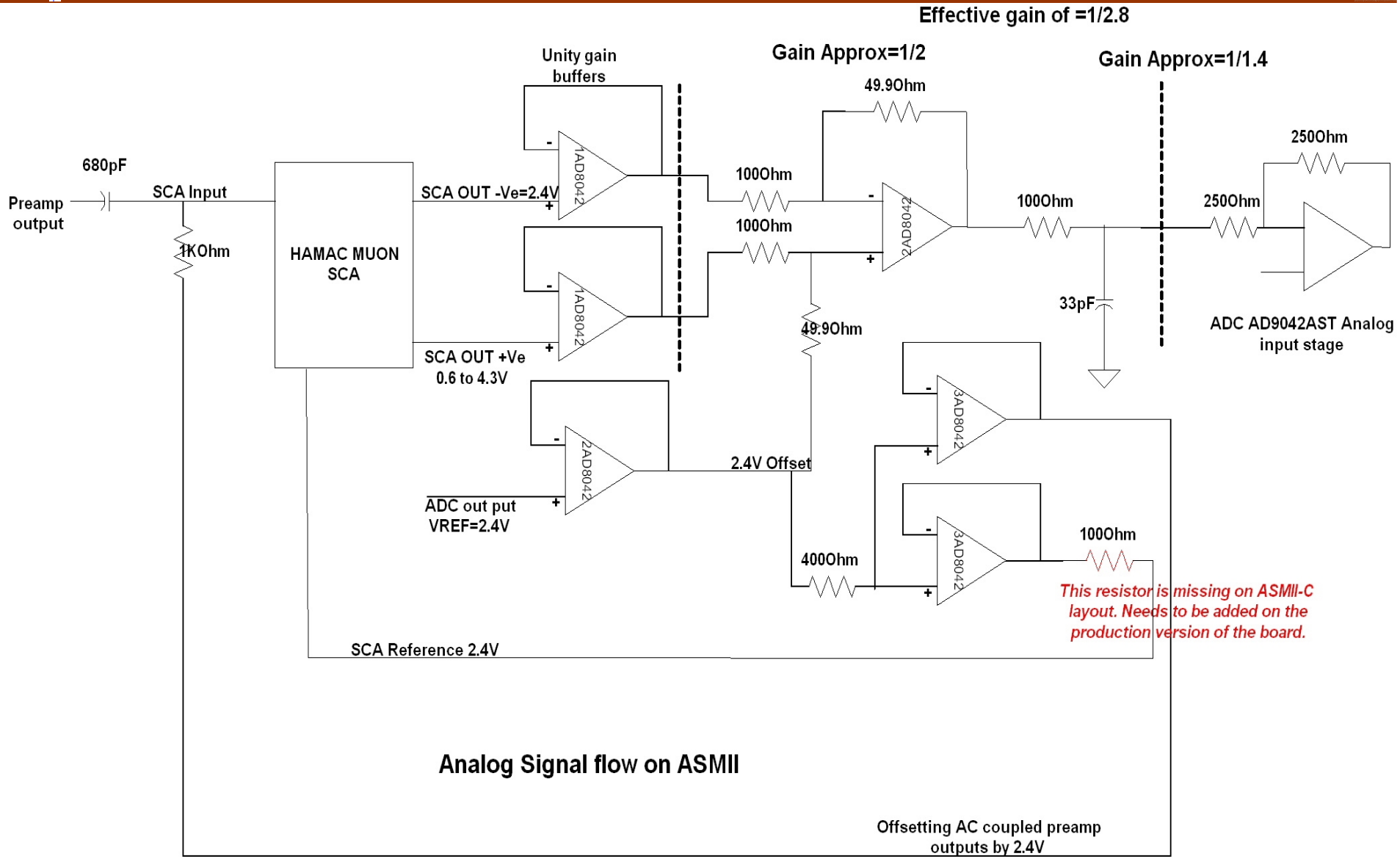
Objectives Met

- Developed SCA Controller
- Tested SCA (muon mode)
- Preamp/SCA interface
- Characterized ADC
- 192 Channels
- Established readout architecture

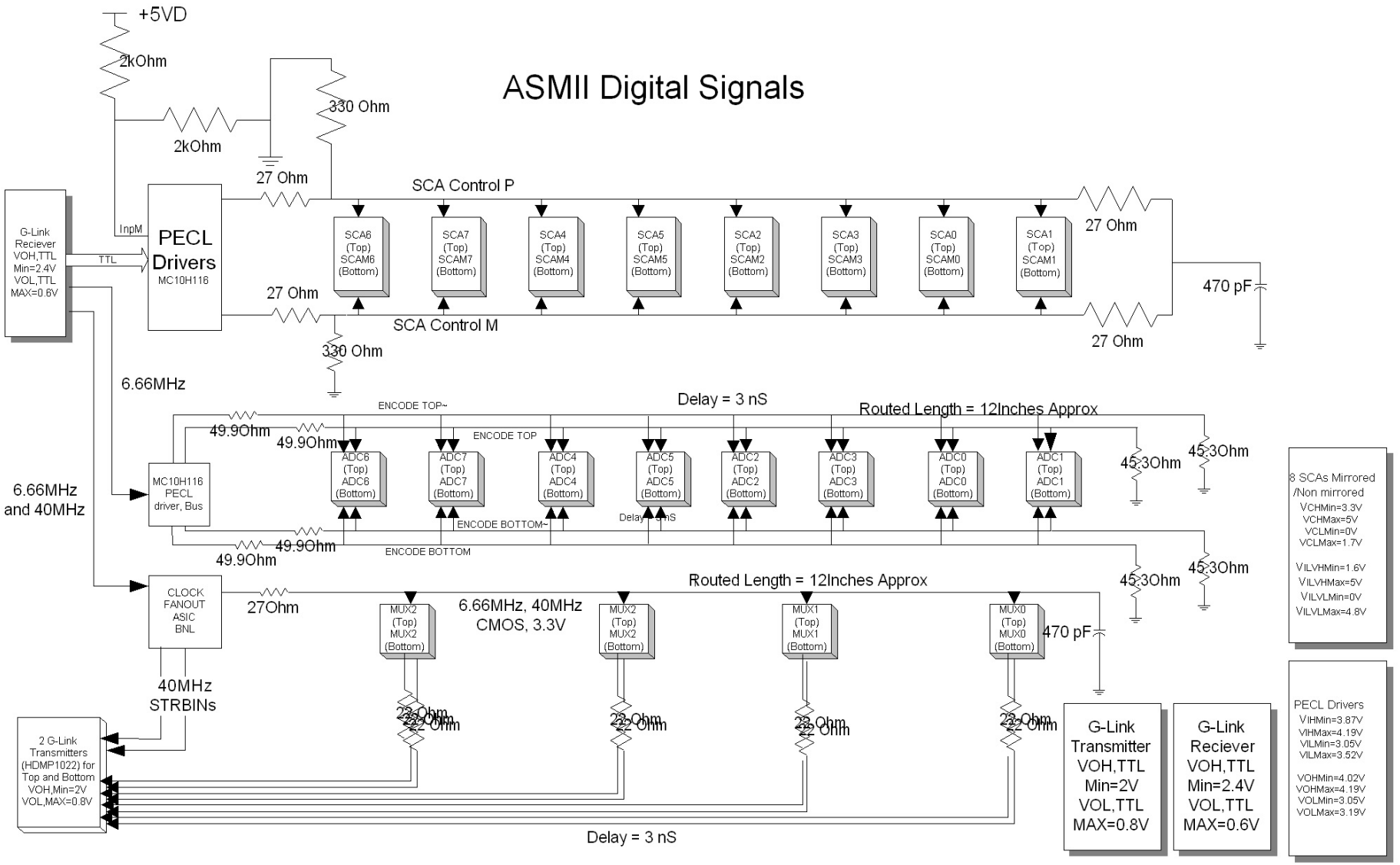
Objectives Met

- Eliminated the FPGA and RAD SOFT buffers
- Reduced noise
- Characterize Noise
- Meets CSC requirements
- Final design

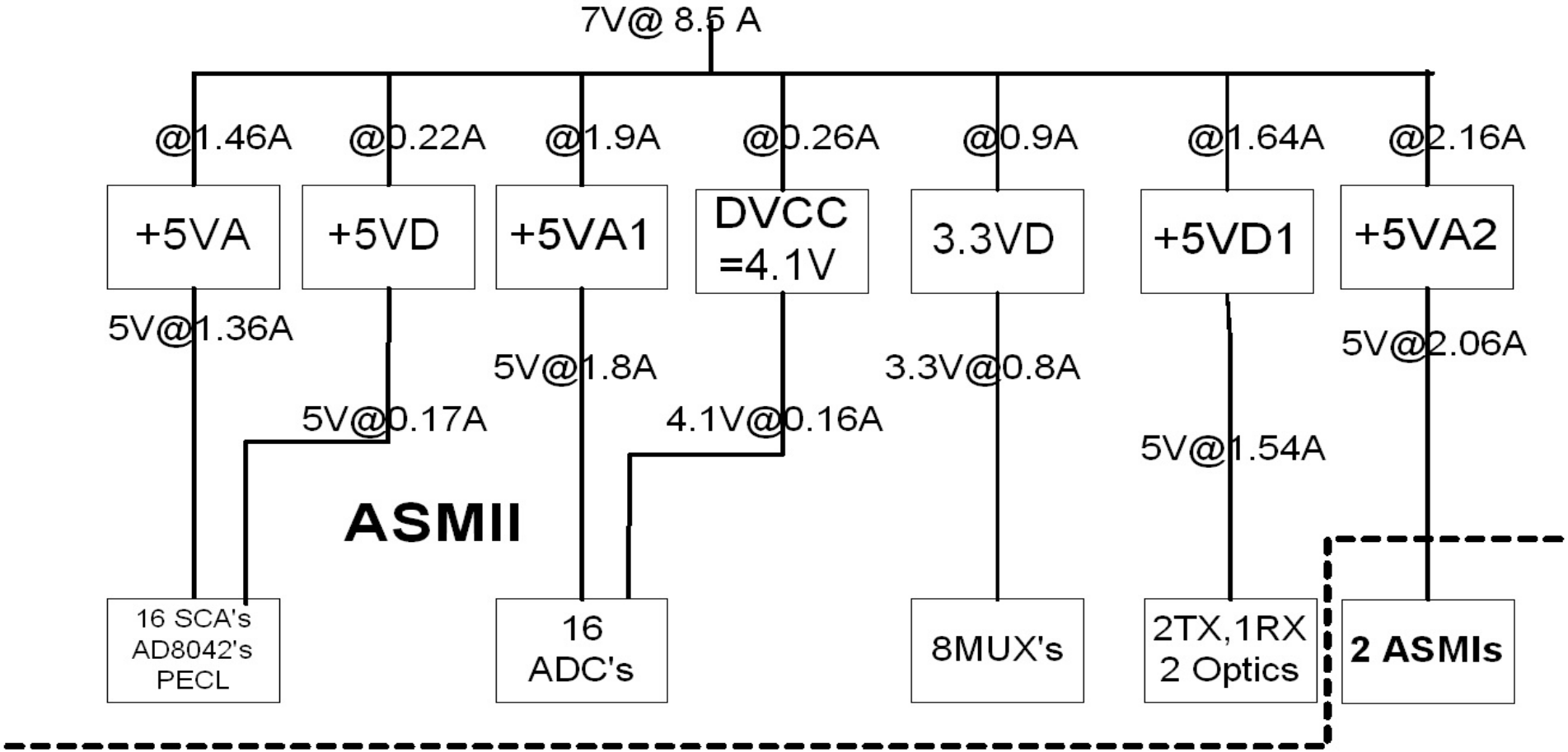
Signal Flow on ASMII



Digital signals on ASMII



Power Distribution on ASMII



Power:
Total:59.43W

CSC ASM PACK Power Distribution

ROD Interface

There are three fiber optic links. 1 from ROD Transition Module (TM) to ASM II carrying 2 links from ASM II to ROD TM Carrying Digitized data

ROD Transition Module has HDMP-1032a Transmitter per ASM II , and 2 HDMP-1034a R

Following table shows the piouts on ASM II and corresponding pins on the ROD End.

Downlink(From ROD TM to ASM II)

	HDMP1032a		HDMP1024
Pin Name	Pin #	ASM II Nai	Pin #
TX[0]	46	RD_CLK	71
TX[1]	47	SD	70
TX[2]	50	RD	69
TX[3]	51	G1	68
TX[4]	52	G0	67
TX[5]	53	WA7	66
TX[6]	54	WA6	65
TX[7]	55	WA5	60
TX[8]	58	WA4	59
TX[9]	59	WA3	58
TX[10]	60	WA2	57
TX[11]	61	WA1	56
TX[12]	62	WA0	55
TX[13]	63	TRIG_DAT	54
TX[14]	2	ADC_CLK	51
TX[15]	3	SCAWCLK	50

Uplink 1(From ASM II to ROD TM RX 1)

	HDMP1022		HDMP1034a
ASM II Nai	Pin #	1034Name	Pin #
LINK1_0	59	RX1[0]	3
LINK1_1	58	RX1[1]	2
LINK1_2	57	RX1[2]	63
LINK1_3	56	RX1[3]	62
LINK1_4	55	RX1[4]	61
LINK1_5	54	RX1[5]	60
LINK1_6	5	RX1[6]	59
LINK1_7	51	RX1[7]	58
LINK1_8	50	RX1[8]	55
LINK1_9	49	RX1[9]	54
LINK1_10	48	RX1[10]	53
LINK1_11	47	RX1[11]	52
LINK1_12	46	RX1[12]	51
LINK1_13	45	RX1[13]	50
LINK1_14	40	RX1[14]	47
LINK1_15	39	RX1[15]	46
TRIGDATA	70	RXDATA	44

Uplink 2(From ASM II to ROD TM

	HDMP1022		HDMP1034
ASMII Nan	Pin #	1034Name	Pin #
LINK2_0	59	RX2[0]	3
LINK2_1	58	RX2[1]	2
LINK2_2	57	RX2[2]	63
LINK2_3	56	RX2[3]	62
LINK2_4	55	RX2[4]	61
LINK2_5	54	RX2[5]	60
LINK2_6	5	RX2[6]	59
LINK2_7	51	RX2[7]	58
LINK2_8	50	RX2[8]	55
LINK2_9	49	RX2[9]	54
LINK2_10	48	RX2[10]	53
LINK2_11	47	RX2[11]	52
LINK2_12	46	RX2[12]	51
LINK2_13	45	RX2[13]	50
LINK2_14	40	RX2[14]	47
LINK2_15	39	RX2[15]	46
TRIGDATA	70	RXDATA	44

TRIGDATA is the pin used to validate the data coming from the ASM II. This pin is driven ASM II ADC's are continuously digitizing. Only those samples corresponding to triggere The pin is activated only when ASM II is transmitting the triggered samples.

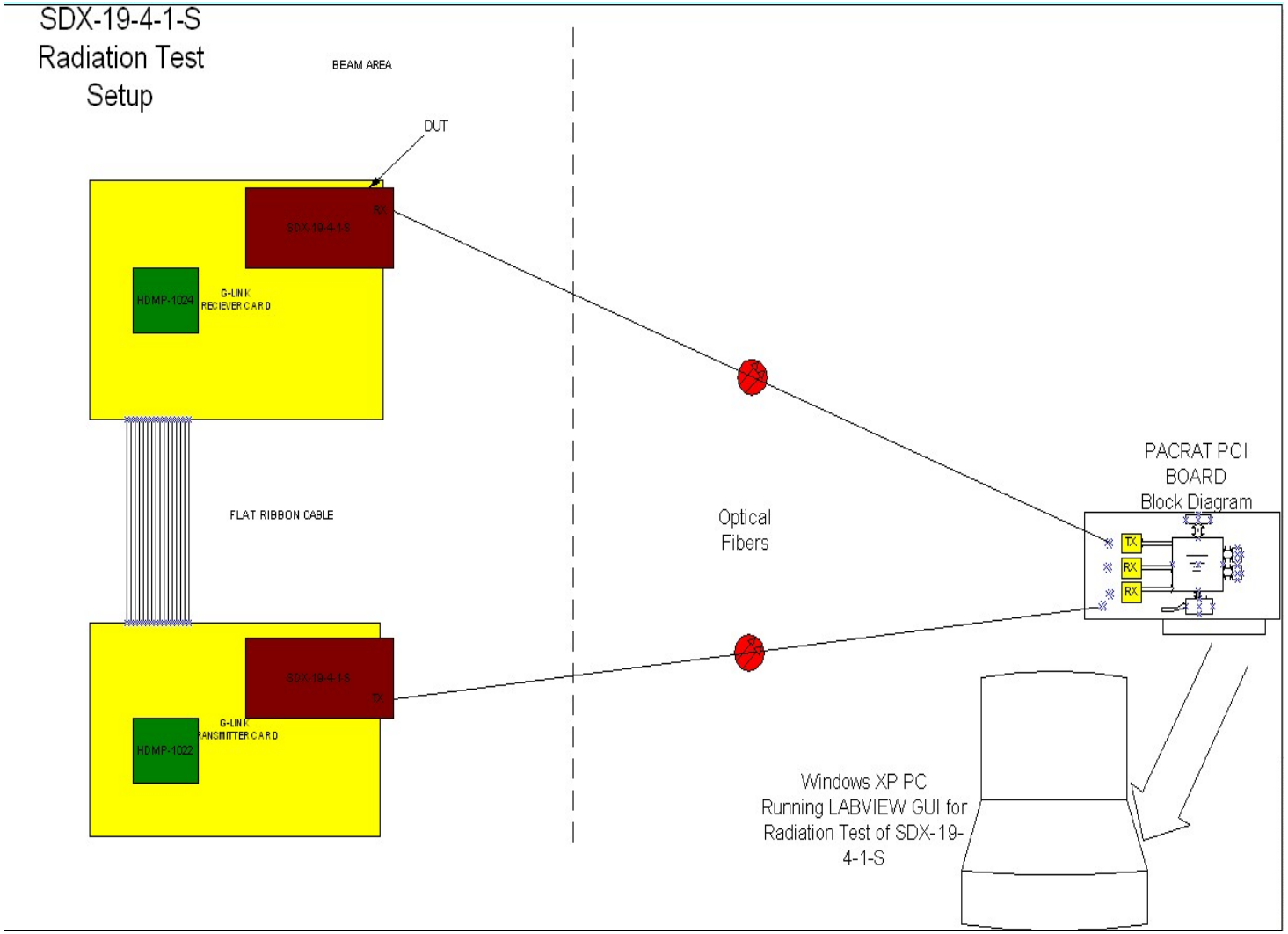
COTs on ASMII

Radiation qualification status		
COTS	Responsible	Status
AD9042 ADC[2]	SMU	Complete
AD8042 Dual opamps[3]	Nevis	Complete
10H116 differential line driver[3]	Nevis	Complete
HDMP- 1022 serialiser[4][5][6]	SMU	Complete
HDMP- 1024 deserialiser[4][5][6][7]	UCI	Complete
SDX-19-4-1-S Optical Transceiver Transmitter[4][5][6]	Nevis	Complete
SDX-19-4-1-S Optical Transceiver Reciever[4][5][6]	BNL	Now

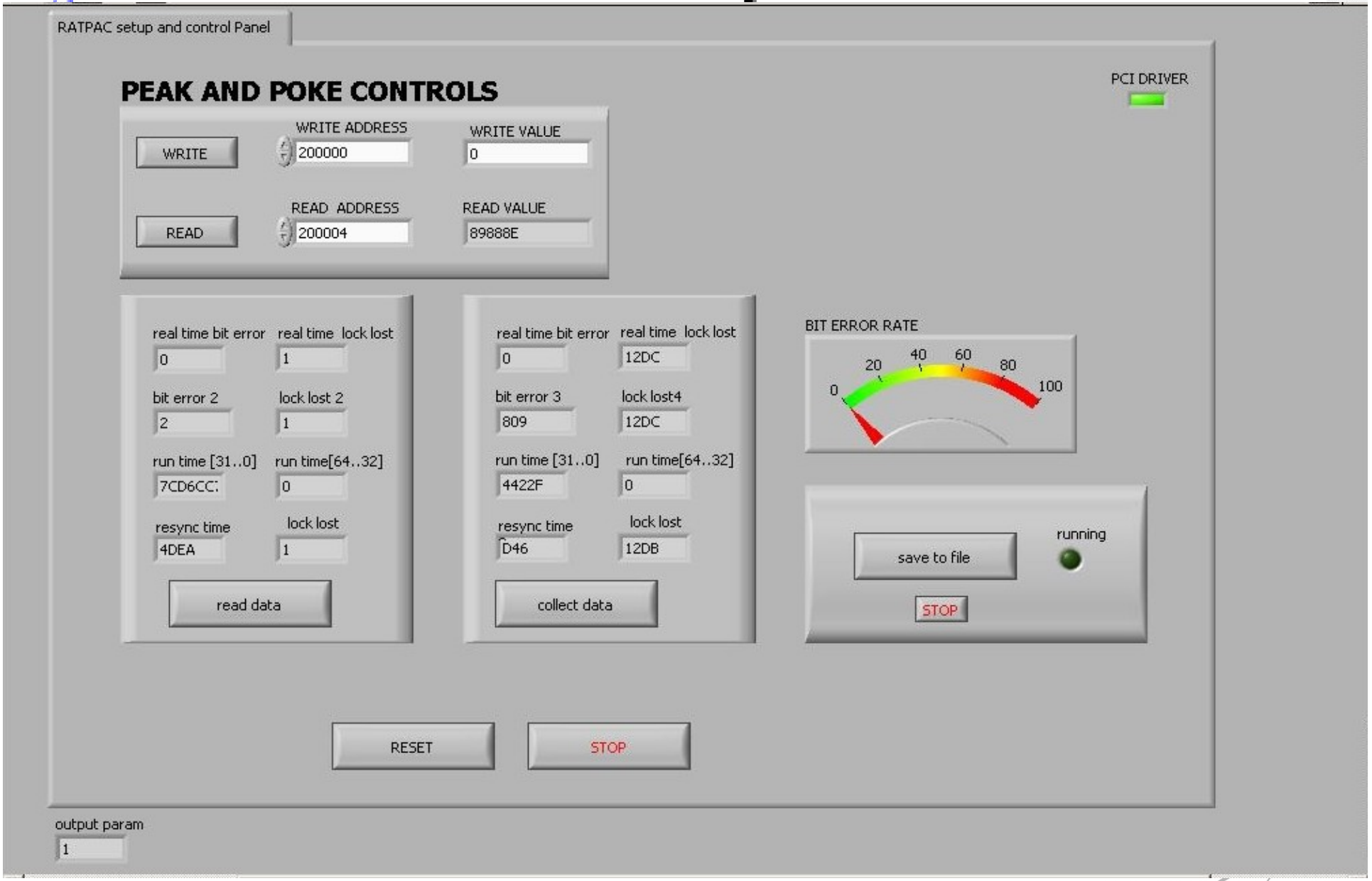
ASICs on ASMII

Radiation qualification status			
ASICs	Technology	Responsible	Status
HAMA/MUON SCA	DMILL	Nevis	Complete
ASM2MUX	HP-0.5u	BNL	Complete
BNL Clock fanout	HP-0.5u	BNL	Same as ASM2MUX

Radiation test setup for Optical Receiver

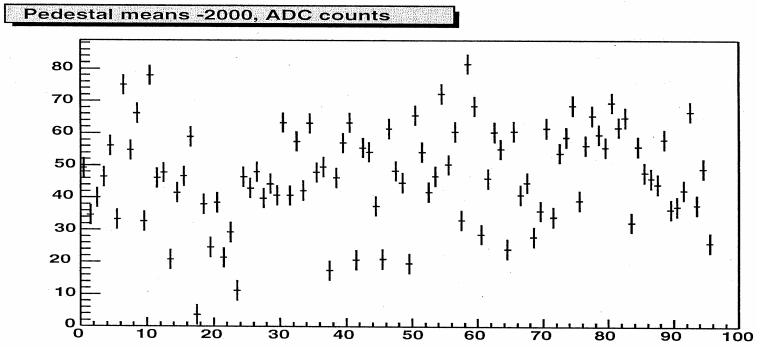


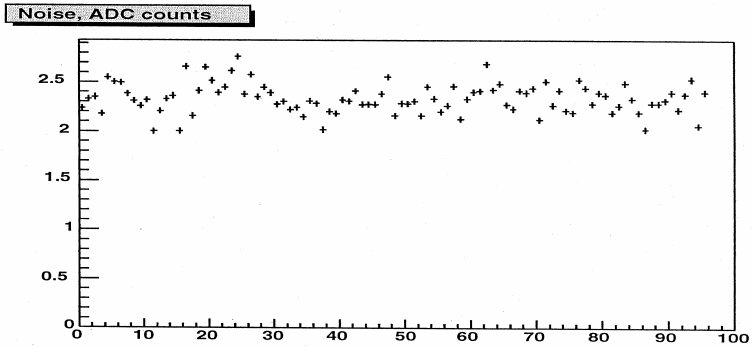
GUI for RX test setup

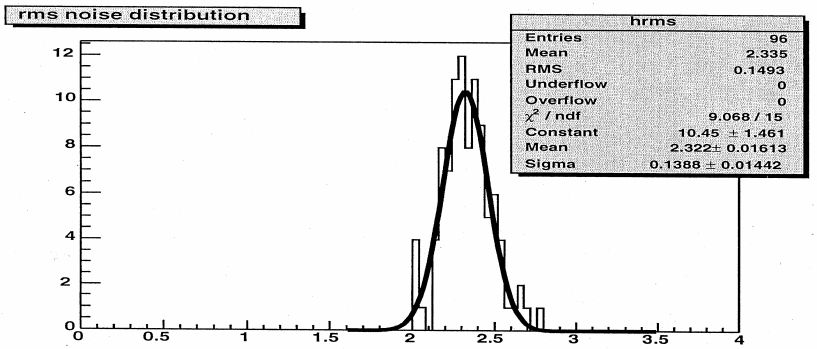


Test Results

ASMII- 5A







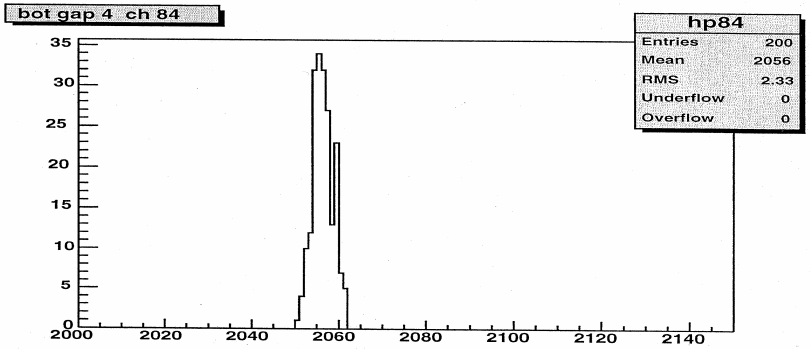
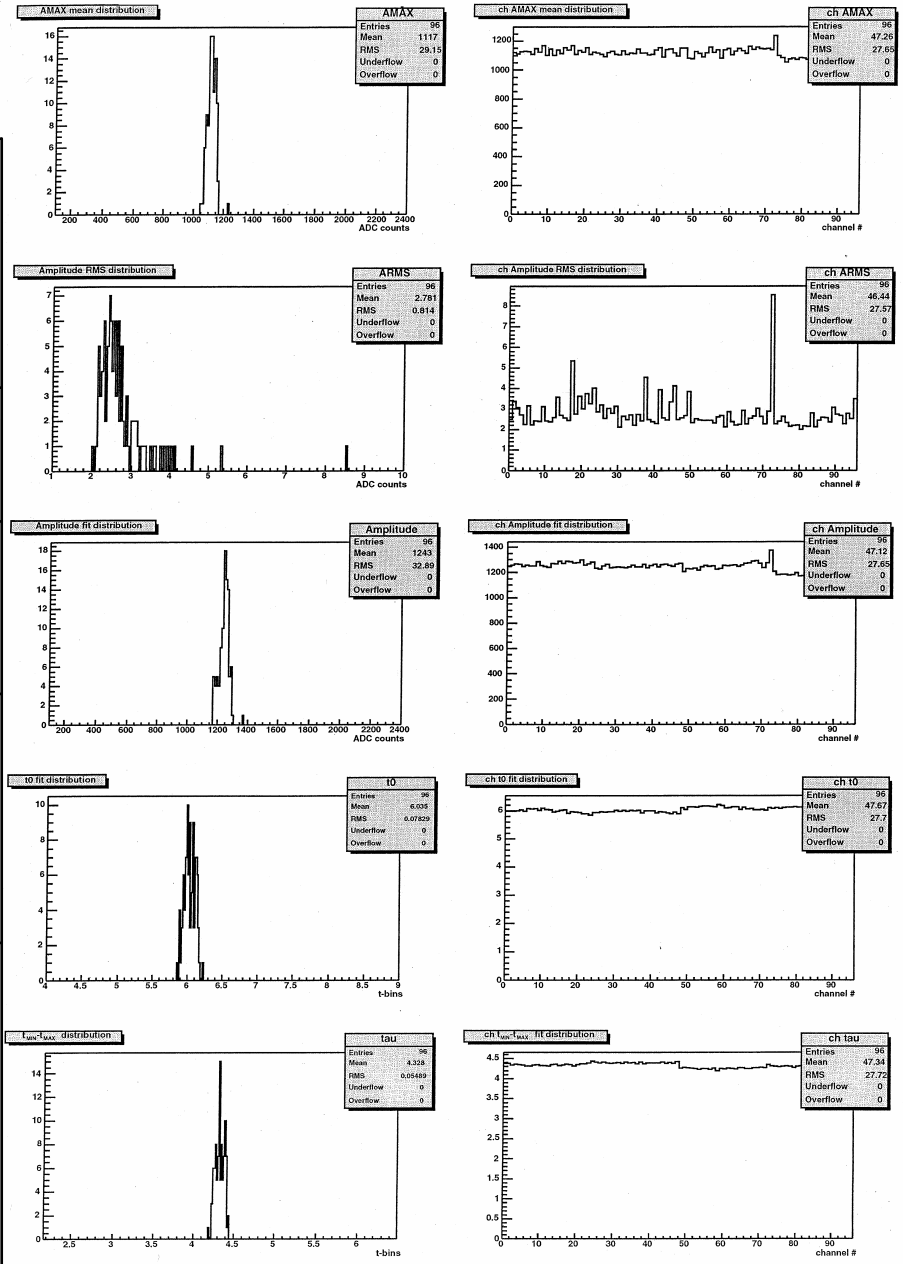


Figure 6a: Pedestal means -2000ADC counts vs 96 channels, averaged over 200 events.	Figure 6b:RMS noise in ADC counts vs 96 channels, RMS of 200 events.
Figure 6c:RMS noise distribution for 96 channels. Mean=2.335, RMS=0.1493, Sigma=0.1388	Figure 6d: Channel number 84 selected at random. Pedestal histogram for 200 events.

Figure 7a: Histogram for 96 channels, of mean of maximum (AMAX) of 4 samples over 200 events. All 96 channels pulsed together with same pulsar.	Figure 7b: AMAX mean distribution vs channel number.
Figure 7c: Histogram for 96 channels of AMAX RMS distribution over 200 events.	Figure 7d: AMAX RMS over 200 events vs channel number.
Figure 7e: Histogram for 96 channels of averages of maximum amplitudes after curve fitting for 200 events.	Figure 7f: Averages of maximum amplitudes after curve fitting for 200 events vs channel numbers.
Figure 7g: Histogram for 96 channels of averages of t0, times of occurrences of maximum in terms of 25ns time bins after curve fitting over 200 events.	Figure 7h: Averages of t0 over 200 events vs channel numbers.
Figure 7i: Histogram for 96 channels of averages of times of occurrences of minimum minus times of occurrences of maximum (tmin - tmax) in terms of 25ns time bins after curve fitting over 200 events.	Figure 7j: Averages of tmin-tmax over 200 events vs channel numbers.



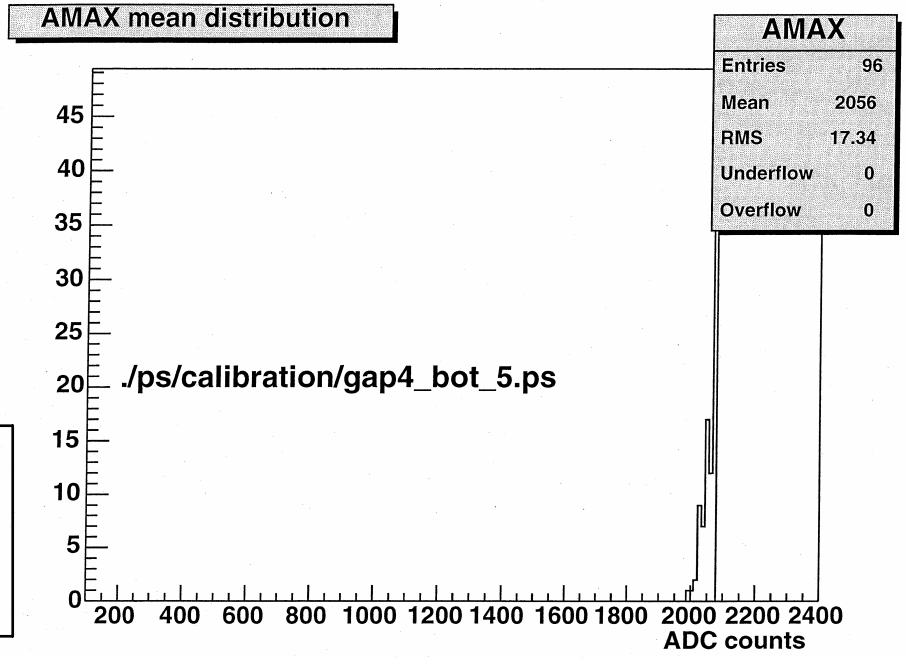


Figure 8a: Histogram for 96 channels of averages of maximum at saturation AMAXsat in ADC counts over 200 events.	Figure 8b: AMAXsat vs channel numbers.

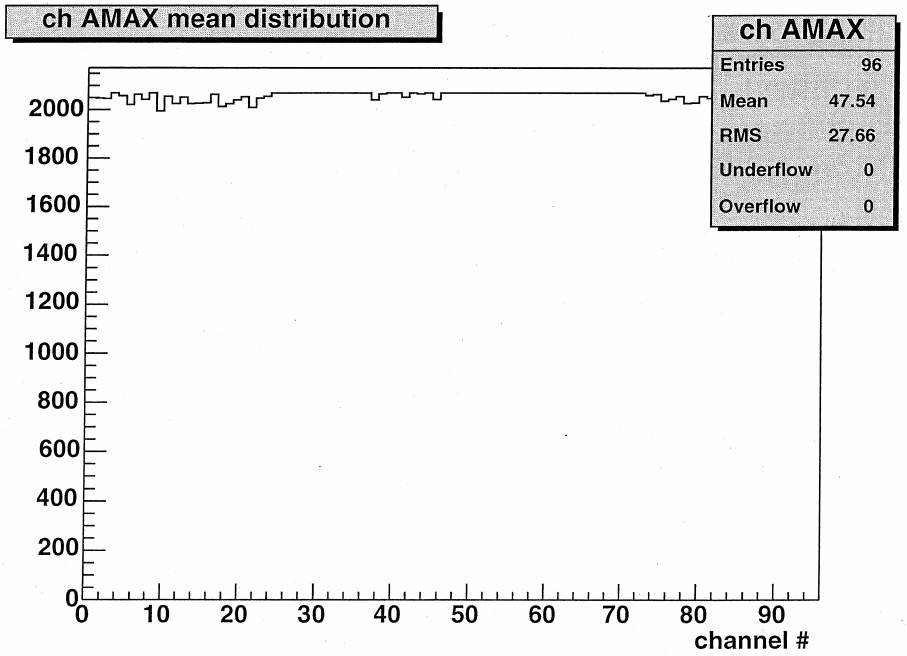
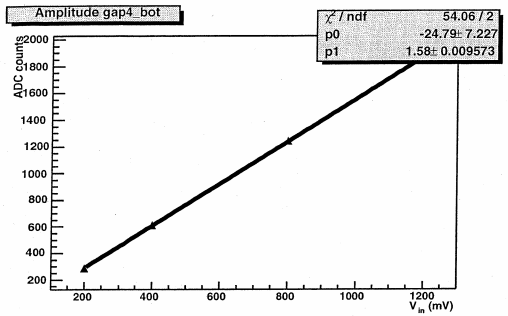
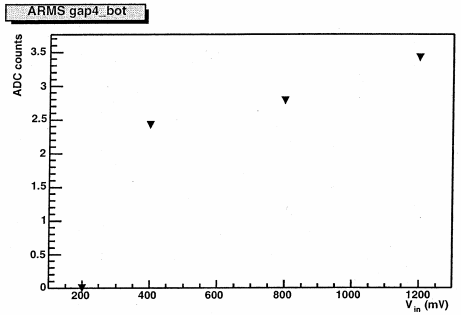
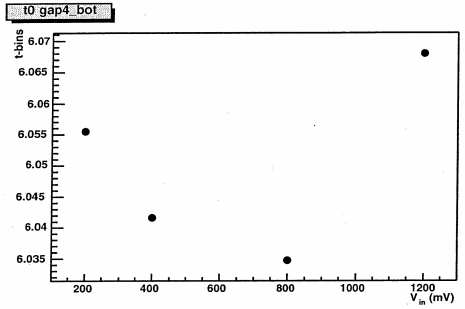
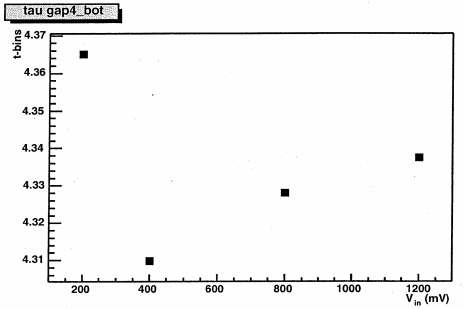


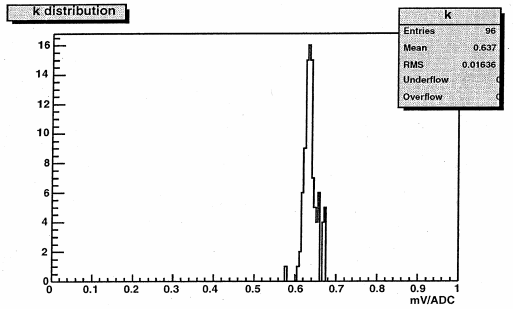
Figure 9a: Average over 50 events for 96 channels of maximum amplitude in terms of ADC counts vs input voltage to the preamps in mV.	Figure 9b: Average for 96 channels of RMS noise in ADC counts over 50 events in the maximum amplitude vs input voltage to the preamps in mV.
Figure 9c: Average time of occurrence of maximum amplitude for 96 channels over 200 events vs input voltage to the preamps.	Figure 9d: Average tmin - t max over 50 events for 96 channels vs input voltage to the preamps.
Figure 9e: Histogram of mV at the preamp output per ADC count for 96 channels.	Figure 9f: mV at the preamp output /ADC count vs channel number.
Figure 9g: Histogram for 96 channels of averages of t0, times of occurrences of maximum in terms of 25ns time bins after curve fitting over 200 events.	Figure 9h: Averages of t0 over 200 events vs channel numbers.
Figure 9i: Histogram of Y intercepts in ADC counts for 96 channels after straight line fit to the individual linearity graph like in figure 9a.	Figure 9j: Y intercepts in ADC counts for individual linearity straightline fits of individual channels vs channel numbers.

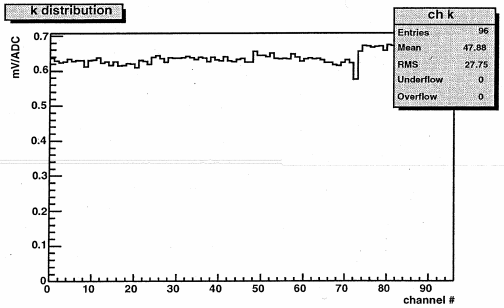


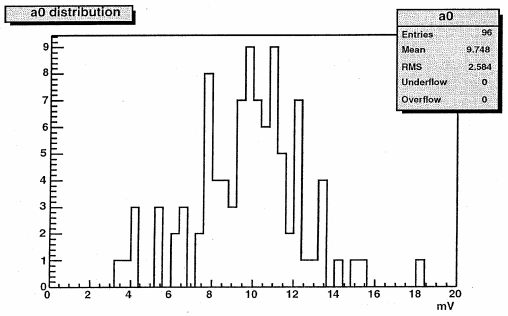


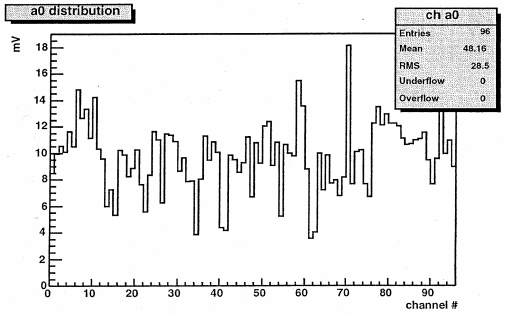








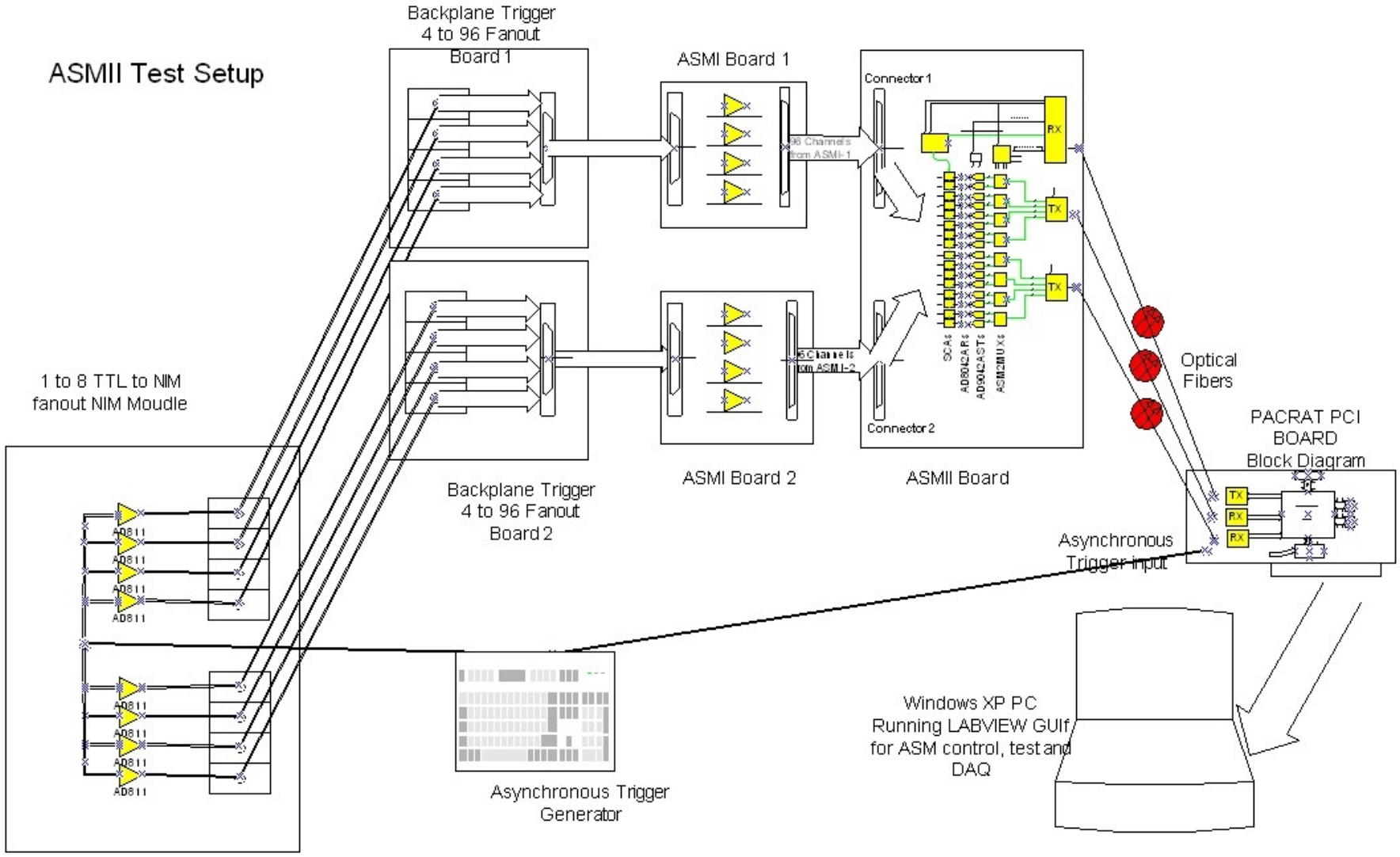




Summary of results

ASMII number	RMS Pedestal Noise Mean in ADC Counts	Sigma	RMS Pedestal noise in electrons	Peak RMS ADC	Fit Amplitude	Channel to channel Spread	t0 /spread, 25nS time bins	ADC count/mV	Number of Bad channels
2A	2.7	0.19	2774	2.87	1260	2.10%	6.23	0.621	1
2B	2.63	0.15	2545	3.06	1336	1.30%	6.34	0.585	2
3A	2.45	0.15	2448	2.74	1297	4.60%	6.31	0.604	1
3B	2.43	0.16	2372	2.8	1343	2.50%	6.3	0.59	None
4A	2.75	0.2	2748	3.47	1298	4.00%	6.18	0.604	2
4B	2.74	0.19	2778	2.93	1259	6.80%	6.26	0.613	2
5A	2.32	0.14	2445	2.78	1243	2.60%	6.04	0.637	None
5B	2.36	0.13	2592	3	1191	2.60%	6.07	0.664	None

Production Test Setup



Production plan: Fabrication

- Board size: 17.125" x 4.804"
- Surface Finish – Electroless Ni, Immersion Au
- 2,907 Holes, smallest hole 0.016" dia
- Test Points - 2,325
- Line Width & Spacing, 0.006" & 0.006"
- Ten (10) Layer, Tetra II Hi-Temp Epoxy 0.072" Thick
- 25 days for fabrication of 180 boards.

Assembly QA/QC

- All components will be mounted and trimmed to IPC 610.
- Components will be baked before assembly
- BNL to supply CADD files and all the components.
- First article of 10 will be produced first and tested.
- The rest of the 170 boards will be assembled and received in batches
- last batch expected in the week of 22nd Aug, 2004.
- Vendor to perform visual inspection

Test procedure

- Before powering on, each board will be tested for possible shorts between GND and between power planes with a multi-meter.
- Boards will be tested with a set of two well characterized ASMIs. Bad channels will be flagged and boards will be repaired in instrumentation, or sent back to the assembler.
- Working boards will be burnt in for 164 hours together with ASMIs.
- A report with test results similar to one presented will be generated on an accepted board.
- Accepted boards will be provided with a bar-coded ID in compliance with the CERN/ATLAS standard.

Schedule

ASMII Board production timeline			
Task	Duration Days	Start	Finish
Fabrication Start	25days	1-Jul-04	26-Jul-04
Parts procurement & kit preperatio	34days	1-Jul-04	4-Aug-04
SDX Transciever radiation testing	1day	TBD	TBD
SDX Transciever procurement	56days	1-Jul-04	26-Aug-04
Assembly Start	28days	27-Jul-04	24-Aug-04
Mount SDX Transcievers	5days	25-Aug-04	30-Aug-04
Recieve 1st articles	14 days	27-Jul-04	10-Aug-04
Evaluate 1st articles	7days	8-Aug-04	15-Aug-04
ASMII Board testing	60days	30-Aug-04	29-Oct-04

Conclusion

- Final ASMII design has evolved over past 3 years through three different versions
- ASMII performance at the system integration test was excellent, and meets all CSC specifications
- Test procedures, quality assurance and control plans have been chalked out.
- ASMII board is ready for production.